REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Final Office Action dated April 4, 2011 and the Notice of Panel Decision from Pre-Appeal Brief Review dated October 5, 2011 have been received and their content carefully reviewed.

By this Response, claims 9 and 30 are amended. No new matter has been added. Claims 1, 8-9, 11-12, 15-27, and 29-30 are pending in the application, with claims 1 and 8 being identified as withdrawn. Reconsideration and withdrawal of the rejections in view of the above amendments and the following remarks are respectfully requested.

In the Office Action, claims 9, 11-12, 15-27 and 29-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cairns et al. ("Cairns1") (U.S. Publication No. 2002/0030653) in view of Cairns et al. ("Cairns2") (U.S. Patent No. 6,268,841), Enami et al. (U.S. Patent No. 5,892,493), Morita (U.S. Patent No. 6,989,810), Nitta et al. (U.S. Patent No. 6,661,402) and Eto et al. (U.S. Patent No. 6,288,697). Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "a multiplexer part performing a time-division on the digital pixel data for a plurality of data lines for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; a level shifter part raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths of the multiplexer part… a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal with respect to a common voltage Vcom; and a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal with respect to a common voltage Vcom… outputting the common voltage Vcom to the corresponding data lines for a disable period of the source output enable signal…" None of the cited references teaches or suggests at least these features of claim 9. Accordingly, claims 9, 11, 12, 15-27 and 29, which depend from claim 9, are thus allowable over the cited references.

In the Response to Arguments section of the Final Office Action at page 4, the Examiner states *inter alia* that the term "common voltage Vcom" is so broad that the teachings of Cairns1 continues to read upon the claim language.

Cairns1 discloses that DACs 21 receive the reference voltage from common reference voltage bus. *See* Cairns1 at paragraph [0061]; Figure 9(b). As previously presented, the reference voltages of Cairns1 correspond to the reference gamma voltages in Figure 5 of the present application, which are different from the common voltage Vcom of the claimed invention. To further clarify the difference between the reference voltages of Cairns1 and the claimed common voltage Vcom, claim 9 has been further amended to include the limitation of "a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal with respect to a common voltage Vcom; and a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal with respect to a common voltage Vcom." Also, the reference voltages in Cairns are supplied to the DACs 21, not to the data lines as required by claim 9. Accordingly, Applicants respectfully submit that the plurality of reference voltages in Cairns1, each having a different voltage level for digital to analog conversion, are clearly different from a single voltage level of the Vcom voltage of the claimed invention.

In the Office Action, the Examiner also asserts at page 6 that "Nitta teaches of that the pixel data sequentially being outputted to positive and negative paths by unit of adjacent pixel data (Fig. 2) using a polarity control signal and an even/odd signal (Fig. 2, item 216)." However, as shown in Fig. 2 of Nitta, item 216 in Fig. 2 is a scan horizontal synchronizing signal that is applied to the scanning circuit 205. *See* also Nitta at 3:1-2. The scanning circuit 205 performs a line-sequential selection for the liquid crystal panel (see *id.* at 2:47-48) and thus does not relate to a modulation of pixel data. Applicants respectfully submit that the scan horizontal synchronizing signal of Nitta are different from both the polarity control signal and the even/odd signal as recited in claim 9.

The Examiner further asserts at page 6 that Nitta discloses "raising a voltage of the time-divided pixel data (Fig. 2, items 228, 229) directly supplied from the positive and negative paths (Fig. 2, items 228, 229) using a level shifter (Fig. 2, item 231)." As recited in claim 9, the time-

divided pixel data is a digital data in the claimed invention. However, assuming *arguedo* that the amplifier 231 in Nitta corresponds to a level shifter, the amplification is performed on analog signals output from the positive and negative DACs 228 and 229 as shown in Fig. 2 of Nitta. DAC stands for Digital to Analog Converter. Therefore, contrary to the Examiner's assertion, Fig. 2 of Nitta fails to disclose the aforementioned features of claim 9.

The Examiner asserts at page 6 that Fig. 2 of Nitta discloses "converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal and converting the other digital pixel of the adjacent digital pixel data inputted to the negative path into a negative pixel signal." This feature of claim 9 is illustrated in Fig. 3 of the present application in which the DAC part 60 including PDAC and NDAC converts the digital pixel data provided by the positive and negative paths PCH and NCH to positive and negative pixel signals. As discussed above, the digital to analog conversion in the claimed invention occurs after the time-divided digital pixel data are level-shifted as recited in claim 30. However, as shown in Fig. 2, the amplification of Nitta is performed after the display data 207 is converted into analog signals by the positive and negative DACs 228 and 229. Therefore, contrary to the Examiner's assertion, Fig. 2 of Nitta fails to disclose the aforementioned features of claim 9.

For at least the foregoing reasons, Applicants respectfully request that the rejection of claim 9 under 35 U.S.C. 103(a) over Cairns1 in view of Cairns2, Enami, Morita, Nitta and Eto be withdrawn.

Claim 30 is allowable over the cited references in that claim 30 recites a combination of elements including, for example, "performing a time-division on a plurality of digital pixel data for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths using a level shifter; converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal with respect to a common voltage Vcom and converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal with respect to the common voltage Vcom… outputting the common voltage Vcom to the corresponding data lines for a disable period of the input source output enable signal of the second horizontal period…" For similar reasons as discussed

with respect to claim 9, Applicants respectfully submit claim 30 is allowable over the cited references.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

By: /Valerie P. Hayes/

Valerie P. Hayes
Registration No.: 53,005
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicant